Page 10, after the heading "CLAIMS" and before the first claim, insert the following:

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--We claim:--

IN THE CLAIMS:

Please substitute amended claims 1-12 as presented below for the same-numbered claims that were pending prior to the filing of this paper. A marked-up version of the amended claims is attached.

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1. (Amended) A coherence controller connected to at least one multiprocessor within a local module, said multiprocessor including a local main memory and a plurality of processors each equipped with a cache memory, said coherence controller comprising:

a cache filter directory including a first filter directory for guaranteeing coherence between the local main memory and the cache memory in each of the processors of the local module;

a complementary filter directory for tracking locations of lines or blocks of the local main memory copied from the local module into at least one external module and for guaranteeing coherence between the local main memory and the cache in each of the processors of the local module and said at least one external module; and

an external port connected to said at least one external module.

2. (Amended) A coherence controller according to claim 1, wherein the cache filter directory includes:

an "n"-bit presence vector where n is a number of multiprocessors in the local module,

an "n-1"-bit extension of the presence vector, where n-1 is a total number of external modules connected to the external port, and

an Exclusive status bit.

3. (Amended) A coherence controller according to claim 2, wherein the external port is connected directly or indirectly to said at least one external module via an external two-point link.

4. (Amended) A coherence controller according to claim 2, further comprising:

"n" control units connected to the n multiprocessors in the local module,

a control unit XPU connected to the external port, and

a common control unit containing the cache filter directory.

5. (Amended) A coherence controller according to claim 4, wherein the control unit XPU and the "n" control units are compatible with one another and use at least substantially similar protocols.

6. (Amended) A multiprocessor module connected to a coherence controller as recited in claim 1.

7. (Amended) A multiprocessor system with a multimodule architecture, comprising:

at least two multiprocessor modules as recited in claim 6, connected to one another directly or indirectly through external ports of coherence controllers located within said at least two multiprocessor modules.

8. (Amended) A multiprocessor system according to claim 7, wherein said external ports are connected to one another through a switching device or router.

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9. (Amended) A multiprocessor system according to claim 8, wherein the switching device or router includes a unit which manages and/or filters data and/or requests in transit between said at least two multiprocessor modules.

10. (Amended) A large-scale symmetric multiprocessor server with a multimodule architecture, comprising:

a plurality of multiprocessor modules, at least a first of said multiprocessor modules including:

a plurality of multiprocessors each equipped with at least one cache memory and at least one local main memory, and

a local coherence controller (64) connected to said multiprocessors and including a local cache filter directory for guaranteeing local coherence between the local main memory and the cache memories in each of said multiprocessors, said local coherence controller connected to at least a second one of said multiprocessor modules,

wherein the coherence controller further includes:

a complementary cache filter directory for tracking a location of memory lines or blocks copied from said first multiprocessor module to the second one of said multiprocessor modules and for guaranteeing coherence between the local main memory and the cache memories in each of the multiprocessors in said first module and the second one of said multiprocessor modules.

11. (Amended) A multiprocessor server with a multimodule architecture according to claim 10, wherein the coherence controller includes:

an "n"-bit presence vector which indicates presence or absence of a copy of a memory block or line in the cache memories of the multiprocessors,

an "n-1"-bit extension of the presence vector which indicates presence or absence of a copy of a memory block or line in cache memories of multiprocessors in the second one of said multiprocessor modules, and

an Exclusive status bit.

12. (Amended) A multiprocessor server with a multimodule architecture according to claim 10, further comprising:

a switching device or router which connects the first multiprocessor module with the second one of said multiprocessor modules, said switching device or router including a unit which manages and/or filters data and/or requests in transit between the first multiprocessor module and the second one of said multiprocessor modules.